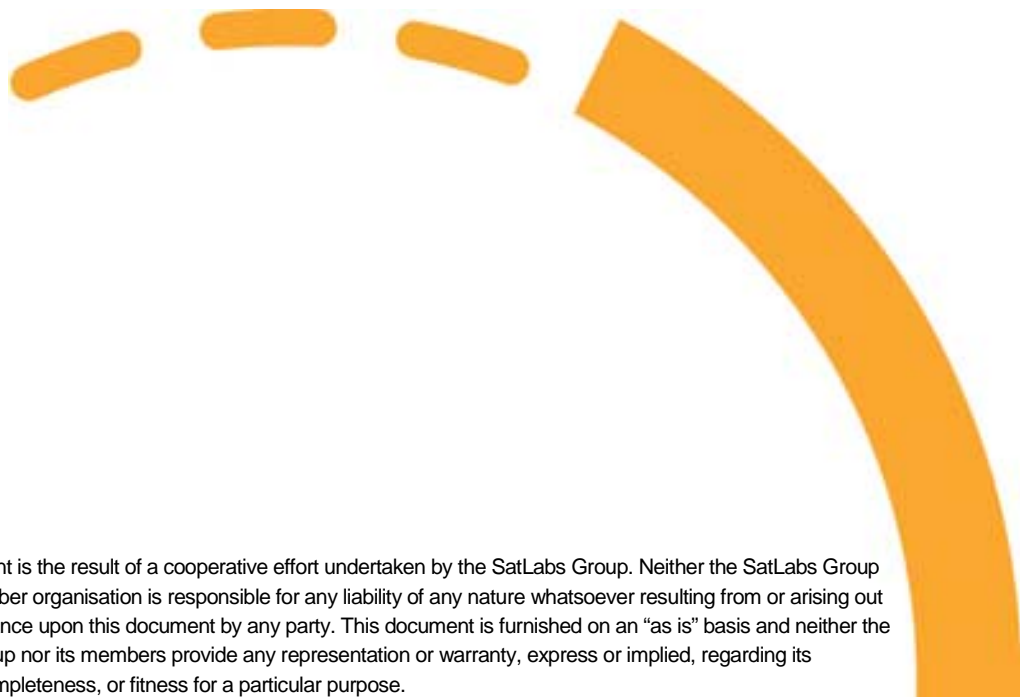




Ku-Band Frequency Upconverter

Version 1.0

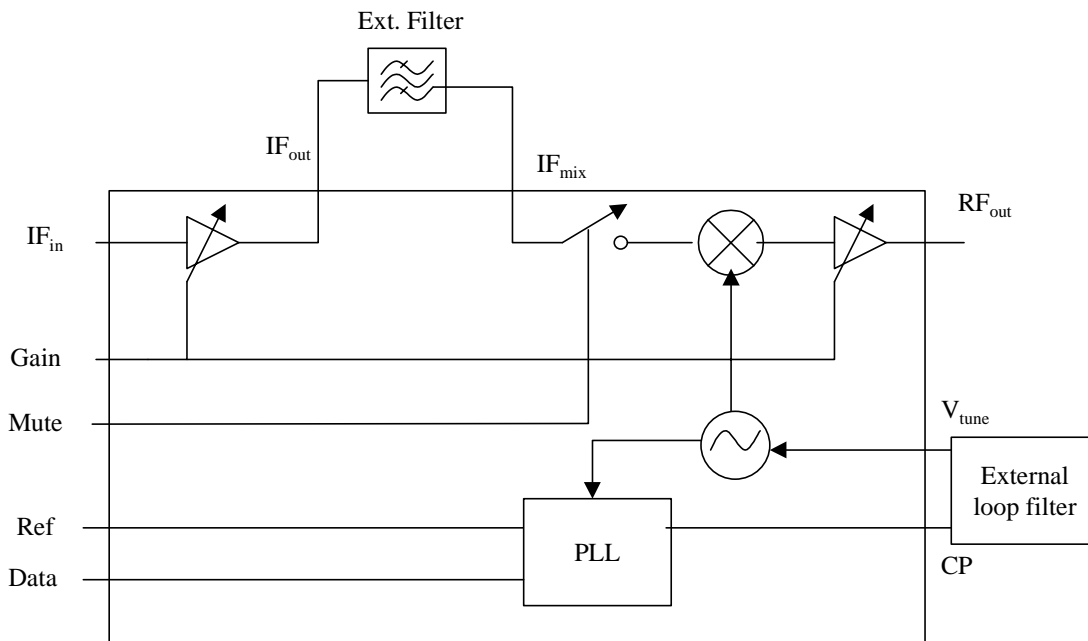


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1. Introduction

This document is a first draft specification for a frequency up-converter chip specifically tailored for Ku-band DVB-RCS. The IC incorporates an IF amplifier line-up with a voltage variable gain control, a mixer, a VCO and PLL circuitry and an output buffer. As an option the circuit should allow for the use of external VCO's. In that case the internal VCO should be disabled. The details of this mechanism are not described in this specification.

A multi-package solution should be considered, if the overall cost or performance can be optimised.



2. pin listing

PIN	Function
IF _{in}	50 Ohm input to IF amplifier
IF _{out}	50 Ohm output from IF amplifier
IF _{mix}	50 Ohm IF input to mixer
Mute	Logic pin, High= Mute on, Low= Mute off
RF _{out}	RF output from mixer, 50 Ohm
Ref	Reference clock input for PLL
Data	data and clock pins for PLL programming (I2C bus or similar). Data pins should include separate pin for lock detect.
IF frequency range	Analog gain control pin 0-5 V
V _{tune}	VCO tuning port
CP	Phase-comparator charge pump output

3. TX IF/DC and reference INTERFACE

Parameter	Min		Max.	Units	Comments
Operating temperature range	-35		75	°C	
DC supply	4.75		5.25	V	
DC current			150	mA	
IF _{in} / IF _{out} / IF _{mix} impedance		50		Ohm	
IF _{in} / IF _{out} / IF _{mix} Return Loss	12			dB	
IF _{in} / IF _{out} / IF _{mix} Frequency Range	950		1450	MHz	
Ref frequency	10		100	MHz	
LO Frequency		(12800) 13050		MHz	(1)
SSB Phase Noise Performance 10 Hz 100 Hz 1 kHz 10 kHz 100 kHz > 1 MHz			-16 -54 -64 -74 -89 -106	dBc/Hz dBc/Hz dBc/Hz dBc/Hz dBc/Hz	(2)
RF _{out} Frequency Range	13.75		14.5	GHz	
Muting attenuation @ any gain control voltage	20			dB	
Settling time Muting OFF->ON/ ON->OFF			100	ns	
Gain control voltage range	0		5	V	Separate Gain control pins for IF and RF may be required. Variable gain at the RF stage can be replaced by constant gain if there is a considerable cost benefit in doing so.
Gain slope		TBD		dB/V	

Gain slope linearity		TBD		dB/V	
Conversion Gain @max gain (From IF _{in} to RF _{out})		25		dB	
Gain @min gain (From IF _{in} to RF _{out})		0		dB	
SSB Noise Figure			15	dB	(3)
Gain Flatness vs. frequency @ any gain setting			1	dBp-p	
Gain stability over temperature (-30°C - +75°C) (Gain control at fixed voltage)			1	dBp-p	
Image rejection			0	dB	
LO residual level at RF output			-10	dBm	measured at max gain
Output P1dB	5			dBm	applies over entire gain range
Spurious response @0 dBm RF output power level					
LO + 2*IF (IF Frequency = 950 MHz)			-67	dBc	(4)
LO + 2*IF (IF Frequency = 1200 MHz)			-57	dBc	(4)
LO + 2*IF (IF Frequency = 1450 MHz)			-47	dBc	(4)

(1) 12800 MHz to be used for terminals transmitting at extended Ku band (13.75-). Whether this function is covered by a separate version of the IC should be clarified.

(2) Phase noise performance as stated in option 1 in Table 13 DVB RCS Guidelines

(3) The relative spectral noise density contribution due to upconverter can be expressed as:

$N_{0(dBc/Hz)} = -IF_{lev(dBm)} - kT_{(dBm/Hz)} + NF_{(dB)}$. For a NF of 15 dB and input IF level of -25 dBm, we obtain $N_0 = -(-25 dBm) - (-173 dBm/Hz) + 15 = -133 dBc/Hz$. This noise level is 27 dB below the DVB-RCS phase noise specification > 1 MHz.

(4) EN 301428 Off-Axis requirements for frequency range 14.75-21.2 GHz. Evaluated for output power of 30 dBm.

4. PLL Section

The PLL should be an integer N- mode circuit with the ability to operate at high phase comparator frequencies for optimum phase noise performance. It is suggested that the reference input should accept input frequencies up to 100 MHz. An R divider should be implemented so that the phase comparator frequency can be programmed by the ODU. The phase-comparator operational frequency should at least be 50 MHz.

A pulse –swallow divider should be implemented for the VCO feedback divider (N-divider)

The PLL should have a charge pump output with fixed or programmable current. The charge pump pin is available at an output pin so that an external loop filter can be employed.

5. VCO

The VCO is assumed to be on-chip. No assumption is made on whether the oscillator is sub-harmonic or not, but the design of the PLL will probably be more straightforward at a fraction of the required LO frequency. Using an external resonator to achieve sufficient Q-value is an option, but it is desirable to keep the complete VCO on-chip.

6. Package

A low-cost surface mount package is assumed.

7. Gain Control

An analogue gain control is desirable for adjusting total transceiver gain, or performing temperature compensation of the power amplifier. The gain response versus control voltage must be well defined in terms of slope and linearity. Although it is desirable to have a variable gain stage at RF as well as at IF, cost considerations may allow a solution where the variable gain stage at RF is replaced by a fixed gain block.

8. Muting function

The mute pin will reduce the conversion gain by a minimum of 20 dB when turned on. Several applications of this function can be envisaged. Firstly the mute function can be employed to reduce noise emissions from inactive terminals, secondly it can be used to turn the transmitter on/off in between bursts being transmitted from active terminals. For the latter the switching time of the muting must be low compared to the symbol rate.

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