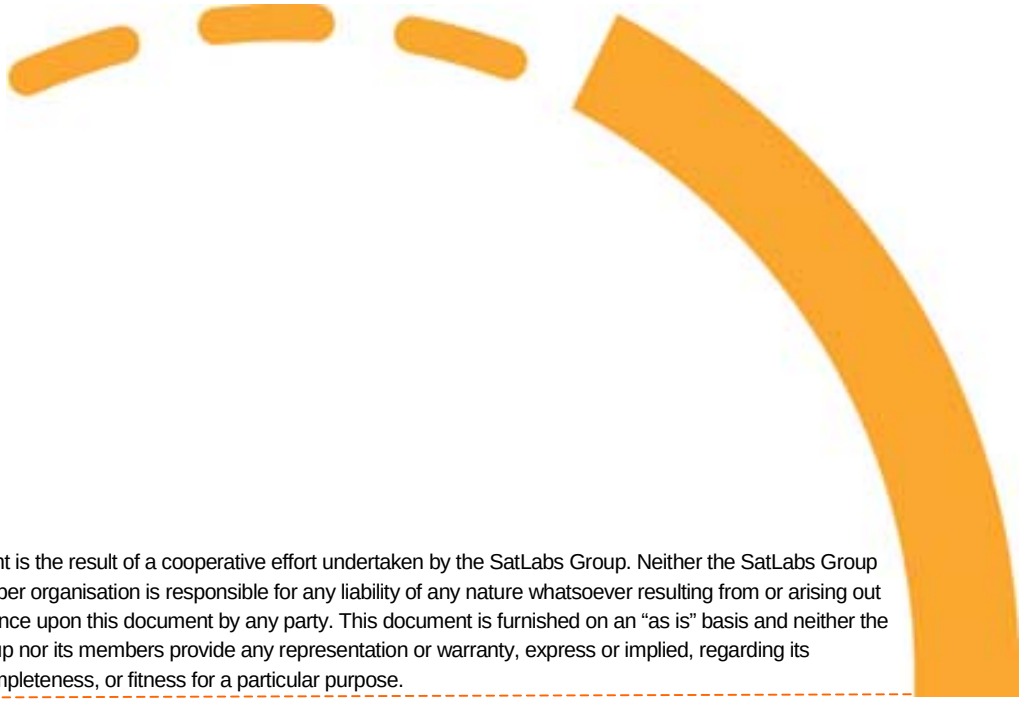
IDU transmit chain
analogue electronics specification

Version 1.0



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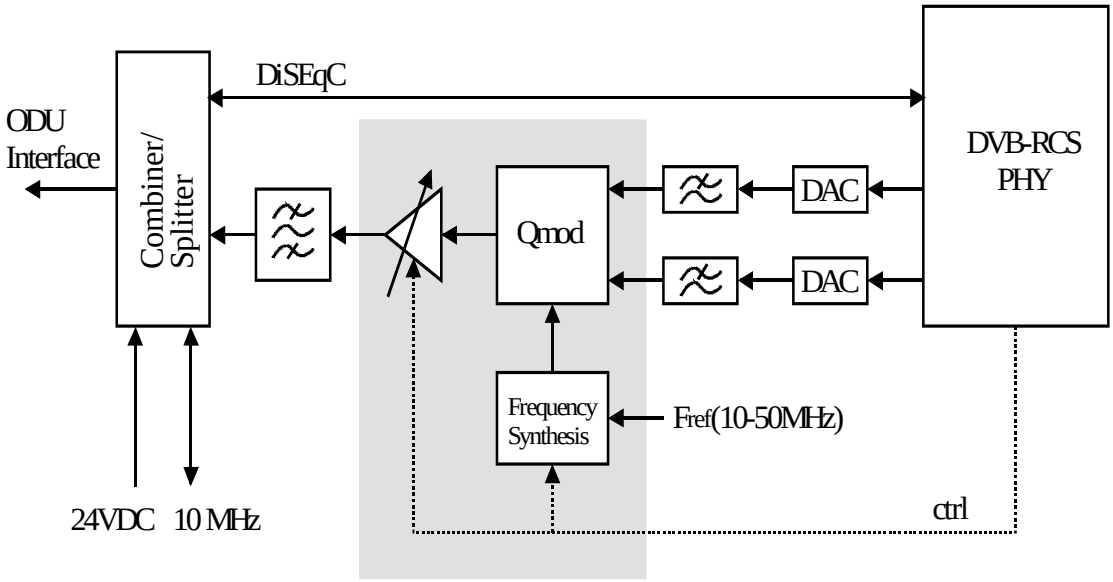
Introduction

The transmit chain is today one of the most costly elements in a DVB-RCS Indoor Unit. While the receiver chain and the processor platform of DVB-RCS IDU can make use of new, lower cost components being developed for the high volume Set-Top box market, there is currently no high volume market driving the development of a low cost TX chip suitable for the DVB-RCS IDUs.

Making a low cost DVB-RCS TX chip available would remove the main obstacle to get the DVB-RCS IDU cost at the same level as the cost of a Set-Top Box.

TX architecture

Figure 0-1: DVB-RCS IDU TX architecture



The figure above shows an example of how the TX chain for a DVB-RCS IDU can be implemented. The DACs and low pass filter can be included in a future DVB-RCS PHY chip. The shaded area shows the modules which are proposed to for integration in a DVB-RCS TX chip, and for which a draft specification is given in the next section.

Proposed specification

No	Parameter	Requirement	
1.	I/Q Input Bandwidth (- 1 dB BW)	num 10 MHz, Preferably 25 MHz or larger	
2.	I/Q Gain Imbalance (over –1 dB BW)	0.3 dB (TBC)	
3.	I/Q Phase Imbalance (over –1 dB BW)	2 deg. (TBC)	
4.	Frequency reference	10-50 MHz (TBC)	
5.	SSB Phase Noise	10 Hz : -28 dBc/Hz 100 Hz : -66 dBc/Hz 1 kHz : -76 dBc/Hz 10 KHz : -86 dBc/Hz 100 kHz : -101dBc/Hz 1 MHz : -118 dBc/Hz	
6.	Output Frequency range (tuning range)	Minimum 950-1450 MHz, Preferably 950-3000 MHz	
7.	Output Frequency step size	50 Hz	
8.	Frequency settling time – slow tuning	The output frequency error must be less than 10 ppb (TBC) within 1s when tuning over the entire frequency range	
9.	Frequency settling time – fast tuning	Option A: The output frequency must be within 100 Hz (TBC) of the wanted frequency within 1 us when tuning over any 40 MHz (TBC) band. The output frequency error must be less than 10 ppb within 50 us (TBC) after tuning over any 40 MHz (TBC) band	Option B: The output frequency must be within 100 Hz (TBC) of the wanted frequency within 100 us when tuning over any 40 MHz (TBC) band. The output frequency error must be less than 10 ppb within 150 us (TBC) after tuning over any 40 MHz (TBC) band
10.	Output Power – Dynamic range	-30 dBm to 0 dBm (TBC)	
11.	Output signal – 1 dB compression	Min.10 dB above max rated output power (TBC)	

No	Parameter	Requirement
	point	
12.	Discrete spurious within output frequency range	-55 dBc (TBC)
13.	Sum of discrete spurious within signal BW (-1 dB BW)	-38 dBc (TBC)
14.	Output power noise density within output frequency range relative to carrier	-128 dBc/Hz (TBC)
15.	Output power step size	1 dB
16.	Output power accuracy	0.5 dB
17.	Carrier suppression when transmitting	-28 dBc (TBC)
18.	Carrier suppression when not transmitting	-50 dBc (TBC)
19.	Processor interface	Preferably asynchronous bus interface for easy connection to CPUs / uControllers / FPGAs / ASICs.
20.	Processor interface speed	All information required for one frequency tuning operation must be transferable within 100 us (TBC)

Target price

When looking on similar analogue receive and transmit chips for high volume markets like the DVB-S receiver market, a target cost of 5 EURO should be achievable. This will typically give a cost reduction of 50-100 EURO for today's DVB-RCS IDU designs for the fast frequency hopping case and 30-50 EURO for the slow frequency hopping case.

Please note that small adjustments to specification may be acceptable if the chip cost can be reduced significantly.

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